

OCT 10 2006 10:38a

Verity Fort Collins

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P. 1



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7590 07/14/2006
AGILENT TECHNOLOGIES, INC.
 Legal Department, DL429
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 P.O. Box 7599
 Loveland, CO 80537-0599
 10/11/2006 RMEBRA1 00000016 10815521

01 FD:1501	1400.00 0P	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
02 PCT:120	300.00 0P	Andrew S. Hildebrand	10031350-1	1566

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Valerie Bakes	(Depositor's name)
Valerie Bakes	(Signature)
October 10, 2006	(Date)

TITLE OF INVENTION: VERIFICATION OF INTEGRATED CIRCUIT TESTS USING TEST SIMULATION AND INTEGRATED CIRCUIT SIMULATION WITH SIMULATED FAILURE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400	\$300	\$0	\$1700	10/16/2006
EXAMINER	ART UNIT		CLASS-SUBCLASS			
DOAN, NGHIA M	2825		716-004000			

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

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(A) NAME OF ASSIGNEE

Verity IPco

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Singapore

Please check the appropriate assignee category or categories (will not be printed on the patent): Individual Corporation or other private group entity Government

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b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

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Date October 10, 2006

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